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<u>L13</u>	L12 and prioritizing near switching	0	<u>L13</u>
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<u>L3</u>	L2 and user-defined	1	<u>L3</u>
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**1. A scalable 160Gb/s switch fabric processor with 320Gb/s memory bandwidth**

Paul, G.; Khan, A.; Zeiger, M.; Cohn, A.; Dramon, D.; Le, D.; Naviasky, E.; Grigoriants, Malobani, I.; Yanuka, I.; Yu, J.; Kung, J.; Gnor, L.; Shiterit, M.; Rozen, R.; Gabe, R.; Ha Wilson, T.; Nguyen, T.; Evans, W.; Hayon, Y.;
Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE 15-19 Feb. 2004 Page(s):410 - 536 Vol.1

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IEEE STD IEEE Standard

**2. ATLAS I: Implementing a single-chip ATM switch with backpressure**

Kornaros, G.; Pnevmatikatos, D.; Vatsolaki, P.; Kalokerinos, G.; Xanthaki, C.; Mavroidi: D.; Katevenis, M.;
Micro, IEEE
Volume 19, Issue 1, Jan.-Feb. 1999 Page(s):30 - 41

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